# Current Sharing Analysis of Interleaved LCLC Resonant Converter

Mojtaba Forouzesh, *Student Member*, *IEEE*, Bo Sheng, *Student Member*, Yang Chen, *Member, IEEE,* Yan-Fei Liu, *Fellow, IEEE*

Department of Electrical and Computer Engineering, Queen's University, Kingston, ON, Canada
Email: m.forouzesh@queensu.ca, bo.sheng@queensu.ca, yang.chen@queensu.ca, yanfei.liu@queensu.ca

***Abstract*— Current sharing in multiphase resonant converters is a serious concern as any small tolerance in the resonant tank components of different phases can lead to a large imbalance in the voltage gain and hence the load current imbalance. An interleaved LCLC resonant converter with four resonant components for wide input voltage range applications is studied in this paper. Because of the sharp voltage gain curve of the LCLC resonant converter, traditional current balancing approaches are not so successful. In this topology, the resonant tank impedances of each phase are tuned by a Switch-Controlled Capacitor (SCC) that is implemented in the resonant tank in both phases resulting in precise load current balancing among paralleled phases. The effect of different imbalance conditions on the interleaved LCLC resonant converter is studied, a minimum operating angle for the SCC circuit is identified and a control strategy is proposed for a reliable current sharing. The performance of the interleaved LCLC converter is validated by both computer simulation and experimental results of a two-phase 1kW prototype with 250V-400V input voltage. Further, a flat high-efficiency profile is achieved with different input voltage conditions over a wide load range.**

***Keywords—Multi-phase resonant converter, interleaved converter, current sharing, current balancing, LCLC resonant converter, switch-controlled capacitor (SCC), GaN HEMTs.***

## I. INTRODUCTION

Resonant converters are one of the widely used power converters in the industry for conversion from common 400 V DC-link voltage to a lower DC bus voltage (e.g. 12 V or 48 V). High interest in resonant converters is due to the unique advantage of soft-switching for all switches that are in a form of Zero Voltage Switching (ZVS) for primary switches and Zero Current Switching (ZCS) for the secondary switches. The latter allows high operating frequency and the utilization of improved magnetics, which leads to increased power density. Furthermore, resonant converters benefit from reduced noise in the system that provides improved electromagnetic interference performance [1] and [2]. In some industrial applications like in data center [3] or Electric Vehicle (EV) auxiliary low voltage onboard charger [4], it is needed for the dc-dc stage to sustain a wide input voltage range operation (e.g. ~250V to ~400 V) to transfer power for a longer time. In [5], it has been demonstrated that the performance of a four resonant components LCLC converter is enhanced in a wide input voltage range operation in comparison to an equivalent LLC resonant converter.

Electrical demand has extremely boosted because of the rapid development of different technologies in recent decades. Hence, the electric power conversion capability should progress with the same pace of the growing need in all kinds of electric power conversion applications (i.e. dc-dc, dc-ac, ac-dc, ac-ac) [6]. For example, in the abovementioned applications, the required voltage level at the load side is usually below 15 V and hence the output current level of power converters should be high (e.g. 100 A) to be able to meet the load requirement. The latter limits the power capability of resonant converters implemented in these applications to around 1 kW [3] and [4]. Therefore, it is needed to connect resonant converters in parallel to dispense current/power stress and hence allow high power implementation. Moreover, by employing phase interleaving the capacitive output filter can be designed with a reasonable value. To take advantage of phase interleaving in frequency-controlled resonant converters, current balancing performance should be thoroughly investigated as the voltage gain of these converters is dependent on the impedance ratio of the resonant tank that can be altered by component tolerances. In multi-phase converters, a slight voltage gain imbalance leads to an unbalanced load current sharing. Unbalanced loading of paralleled phases is a serious issue in interleaved resonant converters as it decreases efficiency and reliability due to the introduced thermal contrast, which can eventually lead to a converter failure.

Up to now, different current balancing approaches including active and passive approaches have been introduced for multi-phase LLC converters [7]-[12]. Various automatic (passive) current balancing methods have been investigated for resonant tanks in [7]-[9]. The passive impedance matching approach is attractive in the current balancing of resonant converters, as usually no additional active/passive components and/or control method are needed. However, the current balancing behavior will be compromised with large resonant component tolerances. Furthermore, phase shedding that is important for light-load efficiency increment cannot be easily implemented with most of the passive current balancing methods.

In [10] an interleaved LLC converter with phase-shift control is introduced for current balancing. This current balancing approach is only applicable to full-bridge topologies

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and it is not so effective for large imbalances as the operation gets too much asymmetrical with large phase shifts. In [11], a current balancing method is implemented on an interleaved LLC converter that takes advantage of adjusted duty-cycle on the phase that carries a higher load share. Although similar to the previous method only a modified control is required here, the primary bridge switches cannot operate with a small duty-cycle to do the current balancing in a wide input voltage range considering large component tolerances. In [12] and [13], current balancing is realized by implementing a switched capacitor/inductor in series with the resonant tank elements to tune the impedance of the resonant tank for voltage gain compensation. This method comes up with an accurate current adjustment between the paralleled phases at the cost of additional electrical components. Nonetheless, the added circuitry does not introduce any switching losses and the extra loss is only related to the device conduction loss that is not significant. Therefore, the overall conversion efficiency is not reduced significantly.

In this paper, a two-phase interleaved LCLC resonant converter is studied for a wide input voltage application. Different from DCX converters with relatively fixed input and output voltages, it is not efficient in wide operating range converters to get small tolerance inductors by implementing PCB windings for the resonant inductors, hence Switch Controlled Capacitor (SCC) approach is a good solution for multiphase LCLC converter that can handle large tolerances. A half-cycle SCC circuit is integrated into the resonant tanks of an interleaved LCLC converter with resonant phase current sensing for each phase. The current balancing behavior of the LCLC tank with the SCC circuit is investigated for wide input voltage range applications considering the tolerances. Moreover, a minimum angle is found for the SCC circuit for reliable operation and current sharing control strategy implementation is discussed in detail. The remaining of this paper is ordered as follows. The analysis of the interleaved LCLC converter is provided in Section II. In Section III, an uncommon imbalance condition is studied, current sharing performance is analyzed, and the proposed control strategy is demonstrated. In Section IV, computer simulation and experimental results are provided, and the paper is concluded in the last section.

## II. The Interelaved LCLC Resonant Converter

LCLC resonant converter for wide input voltage range applications first proposed in [5]. The LCLC converter consists of dual-resonant inductors ($L_r$ and $L_p$) and dual-resonant capacitors ($C_r$ and $C_p$), which in theory is equivalent to an LLC converter with a variable magnetizing inductor.

When the switching frequency of the LCLC converter varies due to different operating conditions, the equivalent magnetizing inductor is altered. This is because the magnetizing impedance is tunable by frequency as the impedance of a series-connected capacitor and inductor changes at different switching frequencies. The LCLC resonant tank elements can be found using the design method described in [5] based on the input and output voltages. The impedance of the equivalent-magnetizing-inductor ($L_{m\_eq}$) can be calculated based on the switching frequency using (1).

$$L_{m\_eq} = L_p - \frac{1}{(2\pi f_s)^2 C_p} \tag{1}$$

The gain of the LCLC tank ($M_{LCLC}$) can be found using the voltage gain of the conventional LLC resonant tank by substituting (1) in place of the magnetizing inductance as follows

$$M_{LCLC} = \frac{1}{\sqrt{\left(1 + \frac{L_r}{L_{m\_eq}} - \frac{L_r}{L_{m\_eq} f_n^2}\right)^2 + Q^2\left(f_n - \frac{1}{f_n}\right)^2}} \tag{2}$$

where the series-resonant frequency ($f_r$), normalized-frequency ($f_n$), the equivalent-resistance transferred to the transformer primary side ($R_e$), and the quality factor are as follows

$$f_r = \frac{1}{2\pi\sqrt{L_s C_s}} \tag{3}$$

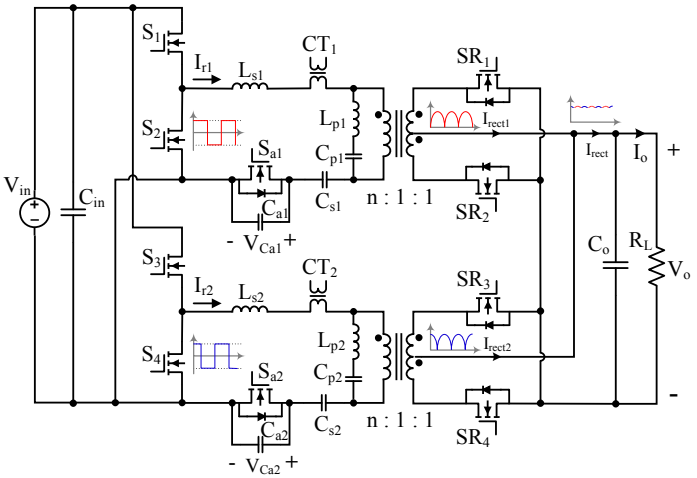
$$f_n = \frac{f_s}{f_r} \tag{4}$$

$$R_e = \frac{8 \times n^2}{\pi^2} \times R_L \tag{5}$$

$$Q = \frac{\sqrt{L_s/C_s}}{R_e} \tag{6}$$

Fig. 1 illustrates the schematic of the interleaved LCLC converter, which was first proposed in [14]. To cancel out any random imbalance with reliable performance, the SCC circuit is implemented in both phases. Switches $S_{a1}$ and $S_{a2}$ are half-wave SCC switches that switch-in and switch-out SCC capacitors ($C_{a1}$ and $C_{a2}$) to tune the impedances to achieve a similar gain for both phases at the same switching frequency. Fig. 2 shows an example of voltage gain compensation at 210 kHz switching frequency operating point for interleaved LCLC converter considering component tolerances for both phases.

Two current-transformers ($CT_1$ and $CT_2$) are utilized for Zero Current Crossing (ZCC) detection that is required to



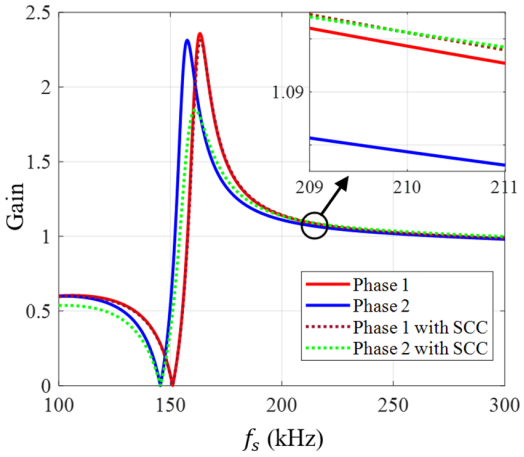



Fig. 2. Voltage gain behavior of the LCLC resonant tank with and without SCC in operation considering different component tolerances on phase 1 and phase 2.

synchronize each phase SCC gate pulses and for the resonant current value measurement/comparison that is required for current balancing and SCC duty-cycle generation (i.e. $\alpha_1$ and $\alpha_2$ operating angles). All the captured information will feed an MCU and appropriate gate pulses will be created for the SCC MOSFETs.

The equivalent capacitance of SCC ($C_{SCC}$) is modulated by SCC MOSFET turn ON angle α and can be expressed as follows

$$C_{SCC} = \frac{2C_a}{2 - (2\alpha - sin2\alpha)/\pi} \tag{7}$$

where $C_a$ is the auxiliary capacitor of the SCC circuit. Then, the resulting total resonant capacitance ($C_r = C_{SCC}||C_s$) can be calculated as follows

$$C_r = \frac{2C_aC_s\pi}{2C_a\pi + 2C_s\pi - 2C_s\alpha + C_s sin2\alpha} \tag{8}$$

where $C_s$ is the series-resonant capacitor of the LCLC tank.

The SCC duty-cycle varies between 0 to 1 that is corresponding to 0 to π of delay angle α for a minimum to maximum total capacitance ($C_r$) in a switching cycle, respectively. The resonant current passes through the SCC capacitor with α=0 bypassing the SCC switch, which creates a series-connected $C_s$ and $C_a$ resulting in a minimum total capacitance. The resonant current passes through the SCC switch with α = π bypassing the SCC capacitor, which creates the maximum total capacitance equal to $C_s$. In other words, $C_r$ can be altered between $C_s$ and a smaller value by switching-in and switching-out $C_a$ to compensate for the resonant component tolerances.

## III. Analysis of Imbalances, Current Sharing Performance, and Control Strategy

### A. Analysis of Imbalances in Interleaved LCLC Resonant Converter

The LCLC tank consists of four resonant elements that have one more inductor compared to the LLC tank. In practice, it is almost impossible to make identical inductors and the resonant capacitors always have some tolerances. As mentioned before, an imbalance between the resonant tank's components of a multi-phase resonant converter can lead to deviation in impedance of the paralleled phases. Any difference in impedances of a frequency-controlled resonant converter causes different voltage gains on paralleled phases, which will lead to unbalanced load sharing between the phases. Therefore, it is critical to investigate the voltage gain of the proposed LCLC converter at the presence of component tolerances.

Using the design procedure provided in [5] for the input values of $V_{in\_min}$=250 V, $V_{in\_max}$=400 V, $V_o$=12 V, $P_o$=500 W, $f_{s\_min}$=170 kHz, $f_{s\_max}$=280 kHz, the following values can be obtained for each phase of the LCLC resonant converter: $L_s$=16 uH, $C_r$ =20 nF, $L_p$ =240 uH, $C_p$ =5 nF and n=18. Unless otherwise stated, these values are used in the rest of the analysis and calculations in this section. To see the effect of the largest component tolerances ±10% variation is considered for the resonant tank components. Moreover, phase 1 is considered as the reference phase in the following analysis.

The effect of tolerance of two components at the same time is considered since only the tolerance of one component cannot reveal abnormal imbalance conditions. Here, the effect of inductor tolerances is only shown as in practice usually a large number of capacitors are paralleled, and the tolerance of capacitors is not large (i.e. usually less than 5%). Hence, the overall effect of capacitor tolerances is not significant. Fig. 3 illustrates the effect of variation in resonant inductance and magnetizing inductance by considering a 10 % decrease/ increase in the value of $L_{s2}$ and $L_{p2}$, respectively. It can be observed that the intersection of two voltage gain surfaces is a curve with variable voltage gain at different frequencies. This is an important phenomenon to consider as with specific tolerances, the voltage gain of one phase can go below or above the other phase's gain at specific frequencies on the intersection curve, which leads to complexity in current sharing for wide input voltage application. Consider Fig. 3(c), if the value of $L_{p2}$ is considerably larger than the value of $L_{p1}$, at low switching frequencies corresponding to low input voltage conditions, the voltage gain of phase 1 is higher than phase 2 (i.e. the orange surface is above the blue surface), and at high switching frequencies corresponding to high input voltage condition, the voltage gain of phase 2 is higher than phase 1 (i.e. the blue surface is above the orange surface). These conditions are likely to happen in practice, so it is important to use an active current balancing on both phases to accurately balance the load share concerning the operation of the circuit. It should be mentioned that any small change in the value of the resonant capacitors can slightly alter the intersection curve in Fig. 3.

To observe the impact of SCC in compensating the voltage gain for both low switching frequency (i.e. 170 kHz) and high switching frequency (i.e. 250 kHz), a 2D plot of the gain curves of interleaved LCLC converter is shown in Fig. 4. As can be observed there is an intersection between the voltage gain of phase 1 and phase 2 which is located below the resonant frequency. Based on Fig. 3, this scenario can only happen when at least two components have tolerances in the opposite

direction. This case is more likely to happen in practice as the proposed interleaved LCLC resonant converter has four resonant elements on each phase and there is no control on the component tolerances. As can be observed in Fig. 4, the SCC circuit in phase 2 is compensating for the gain difference at low switching frequency with $\alpha_2$=123° while the other phase SCC is disabled (i.e. $\alpha_1$=180°), and the SCC circuit in phase 1 is compensating at high switching frequency with $\alpha_1$=147° while the other phase SCC is disabled (i.e. $\alpha_2$=180°).

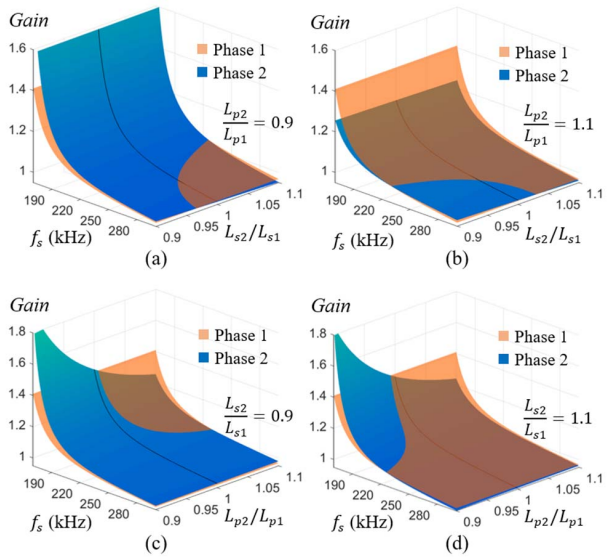



Fig. 3. A 3D illustration of the effect of component tolerances on the voltage gain of the interleaved LCLC converter, (a) ±10% tolerance in $L_{s2}$ while $L_{p2}$<$L_{p1}$, (b) ±10% tolerance in $L_{s2}$ while $L_{p2}$>$L_{p1}$, (c) ±10% tolerance in $L_{p2}$ while $L_{s2}$<$L_{s1}$, and (d) ±10% tolerance in $L_{p2}$ while $L_{s2}$>$L_{s1}$.

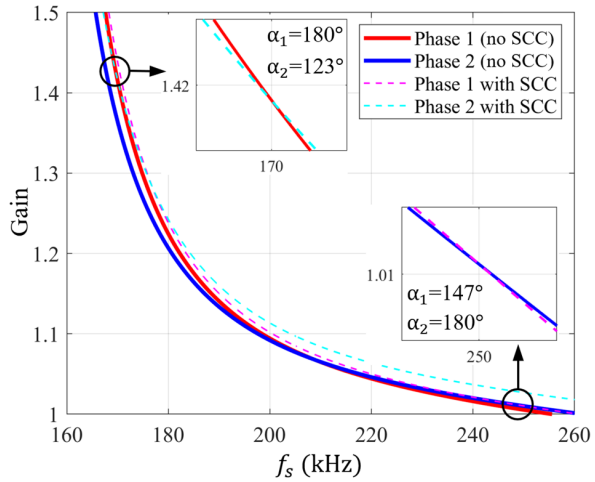



Fig. 4. Performance of SCC circuit with $C_a$=20 nF in the presence of an intersection in voltage gain curves at below resonant frequency.

## B. *Analysis of Current Sharing Performance*

When the load level varies in the LCLC converter both the voltage gain curve and the resonant current alter. Therefore, the Root Mean Square (RMS) current through the series-resonant inductor ($I_{r\_RMS}$) can be investigated to observe the effect of varying delay angle α on the current balancing. For simplicity in calculations, a near-resonant frequency operation ($f_s = f_r$) is considered with a purely sinusoidal resonant current. Hence, the resonant current through the LCLC tank can be expressed as follows

$$i_r(t) = \sqrt{2} I_{r\_RMS} \sin(2\pi f_s t - \phi) \tag{9}$$

The current through the magnetizing inductor can be expressed as follows

$$i_m(t) = \begin{cases} -I_{m\_max} + \dfrac{nV_o}{L_{m\_eq}} t \\ I_{m\_max} - \dfrac{nV_o}{L_{m\_eq}} (t - \dfrac{T}{2}) \end{cases} \tag{10}$$

where the maximum value of the magnetizing current is found in (11).

$$I_{m\_max} = \frac{nV_o T}{4L_{m\_eq}} \tag{11}$$

The RMS current through the series-resonant inductor can be found in (12), which is calculated by subtracting the circulating current through the magnetizing inductor from the resonant inductor current.

$$I_{r\_RMS} = \frac{V_o \sqrt{4\pi^2 + n^4 {R_L}^2 \left(\dfrac{1}{L_{m\_eq} f_s}\right)^2}}{4\sqrt{2} n R_L} \tag{12}$$

When the delay angle α varies on any phase, the total resonant capacitance of that phase alters, and subsequently the voltage gain changes leading to a variation in the resonant current. Using (2), the RMS value of the resonant current related to the LCLC resonant tank components can be found as in (13).

Generally speaking, small α angles with a small SCC capacitor can vary the total resonant capacitance by a large amount causing a considerable variation in the half-cycle resonant frequency, which can increase the power losses due to unbalanced asymmetrical operation of the LCLC resonant converter. Hence, small values of α must be avoided in practical

$$I_{r\_RMS} = \frac{V_{in} \sqrt{4\pi^2 + n^4 {R_L}^2 \times \left(\dfrac{1}{L_{m\_eq} f_s}\right)^2}}{8\sqrt{2} n^2 R_L \sqrt{\left(1 + \dfrac{L_s}{L_{m\_eq}} - \dfrac{L_s}{L_{m\_eq}} \times \dfrac{1}{4\pi^2 L_s C_r f_s^2}\right)^2 + \dfrac{L_s}{C_r} \times \left(\dfrac{\pi^2}{8n^2 R_L}\right)^2 \left(2\pi\sqrt{L_s C_r} f_s - \dfrac{1}{2\pi\sqrt{L_s C_r} f_s}\right)^2}} \tag{13}$$

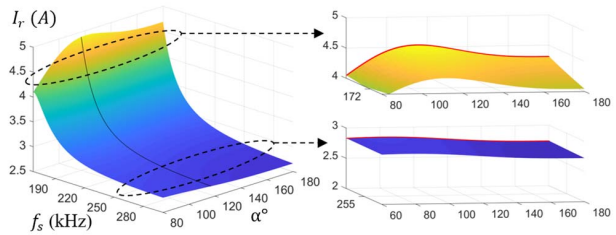



Fig. 5. A 3D plot for the variation of the resonant current versus the variation in switching frequency ($f_s$) and delay angle α (with $C_a$=20 nF).

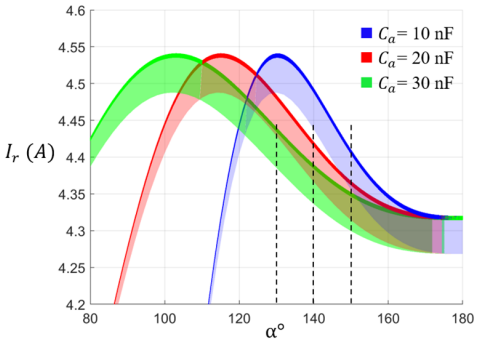



Fig. 6. A 2D plot for the variation of the resonant current versus the variation in delay angle α at fixed 170 kHz switching frequency with different $C_a$ values.

implementation. A 3D plot for the variation of the resonant RMS current versus the variation of switching frequency and delay angle α is shown in Fig. 5. As can be observed the variation of resonant current RMS value is maximum when the input voltage is low (i.e. switching frequency is low). Moreover, by reducing the α angle from 180°, the resonant current first increases to a peak value and then decreases sharply. To have reliable performance, a unidirectional change of current is always sought from the SCC circuit. Hence, it is desirable to set the minimum limit of SCC operating range to the angle corresponding to the peak resonant current ($\alpha_{min}$). In practice, an α value smaller than but close to 180° might be selected for the maximum α limit (e.g. $\alpha_{max}$=170°), since the variation of resonant capacitance and hence balancing is slow at high α angles close to 180°. It should be noted that finding $\alpha_{min}$ from (13) leads to overdesign as this equation is based on first harmonic approximation (FHA) and the actual lower limit would be smaller than what is observed in Fig. 5.

In Fig. 6 different values of the SCC capacitor are used and it is clear that the peak value of resonant current is not changing, however, the α angle corresponding to this peak value is changing (i.e. $\alpha_{min}$). When $C_a$ is reduced, $\alpha_{min}$ is increased and the slope of current change gets steeper. This phenomenon leads to limited operating grange and reduced current sharing accuracy of the SCC circuit.

### *C. Proposed Control Strategy for the Interleaved LCLC Resonant Converter*

Key operational waveforms of the interleaved LCLC converter with SCC current sharing is shown in Fig. 7. It is

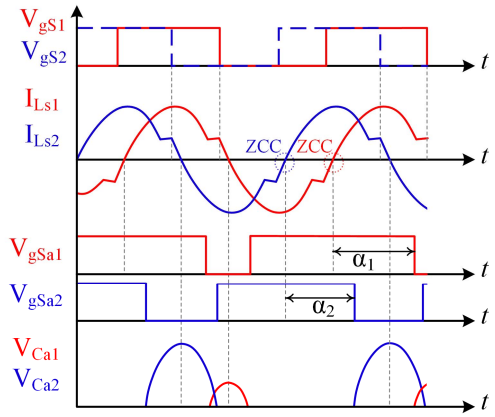



Fig. 7. LCLC converter key operational waveforms with SCC.

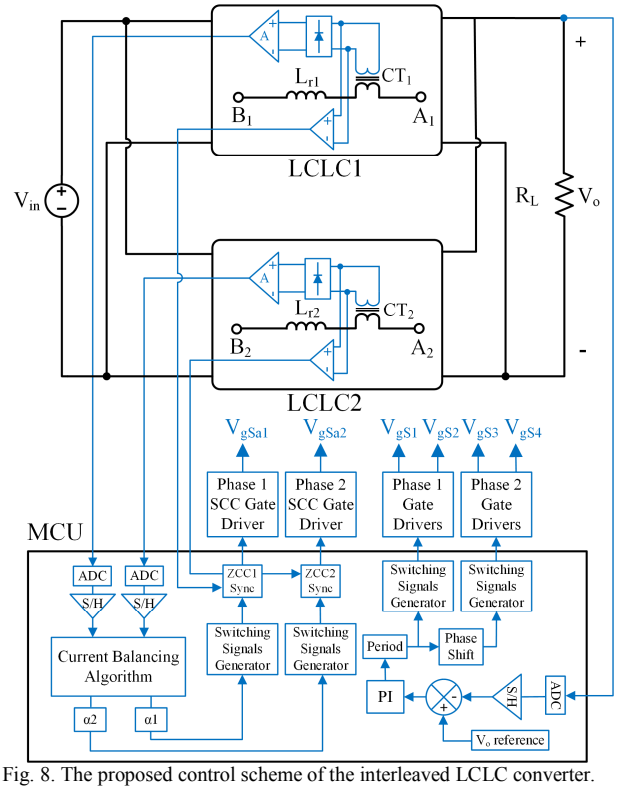



Fig. 8. The proposed control scheme of the interleaved LCLC converter.

assumed that the load part share in phase 2 is smaller than phase 1 in the drawn operating condition and hence a smaller SCC delay angle is needed on phase 2 to compensate for the current difference (i.e. $\alpha_2$ smaller than $\alpha_1$). As it is shown in Fig. 7, it is required to monitor the Zero Current Crossing (ZCC) instants of the resonant current for both phases to properly turn ON the SCC switches.

Fig. 8 shows the digital control implementation of the interleaved LCLC resonant converter. The LCLC tank resonant current is sensed via a current-transformer on each phase to realize the load balancing between the paralleled phases. Then, according to the proposed control algorithm that is illustrated in

Fig. 9, the appropriate command for increasing or decreasing delay angle α of each phase is calculated in the MCU. In practical implementation, load level measuring current-transformer can also be used to synchronize the turn ON of the SCC switch with ZCC of each phase. Furthermore, the output voltage level is regulated by a frequency-controlled PI loop that is working separately from the current balancing function. A complete flowchart of the current balancing algorithm is illustrated in Fig. 9.

As mentioned before, it is favorable to first increase delay angle α of the larger current carrying phase to its maximum value, and then decrease delay angle α of the other phase. Different steps of the current balancing control are as follows:

1) Initially, the α angles of both phases are set at the maximum. If there is an imbalance in the system, the load sharing will be unbalanced.
2) Then, the current share of both phases is measured via the resonant current and the absolute value of difference between the sensed currents is checked to be larger than a specified threshold (ε). The process of balancing will not start if the sensed currents are close enough, and the process of reading and comparing continuous.
3) When the balancing starts, the current of both phases is compared to see which phase has a larger current. Then, if the current of phase 1 is larger than the current of phase 2, the SCC angle of the larger current phase should be checked to be at maximum, if not, the α angle of that phase should be increased until getting to the maximum value.
4) After the SCC angle of the higher current phase gets to the maximum value, the SCC angle of the other phase should reduce until the difference between the resonant current of both phases gets smaller than ε. At this point, the α will not change further until the absolute current difference is larger than ε.

## IV. Simulation and Experimental Results

Fig. 10 illustrates a photograph of the laboratory prototype of 1 kW interleaved LCLC resonant converter. The parameters used in the laboratory prototype are mentioned in Table I. In this prototype, TO-220 enhancement-mode GaN HEMTs are used for the primary side bridges, and for consistency the same package of the switch is used for the SCC MOSFETs and Synchronous Rectifiers (SRs). Moreover, reliable performance of switching devices is observed with TO-220 packages in the prototype, which is considered similar to surface mount counterparts but with easier thermal management. Only forced air cooling is used in the testing and no heat sink was used for switches. It should be mentioned that the inductors are deliberately wound with different values to count for the imbalance condition.

A detailed computer simulation setup with digital control implementation is built in the PSIM environment using the parameters of the experimental setup. Fig. 11 illustrates both steady-state simulation and experimental results of resonant

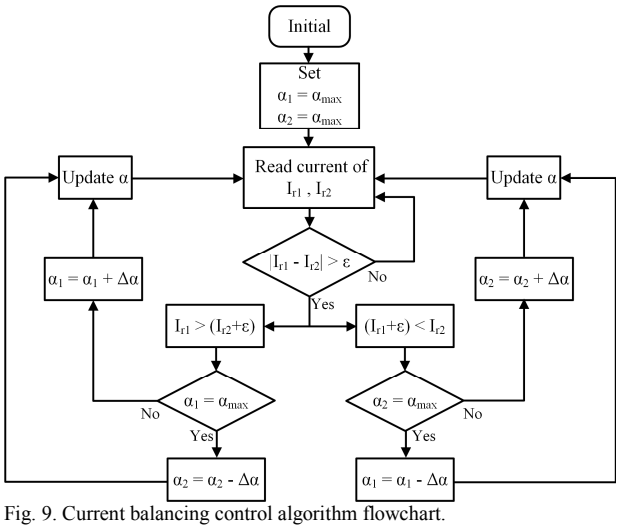


Fig. 9. Current balancing control algorithm flowchart.

TABLE I. The Parameters Used in the Prototype

| Description | Value |
|---|---|
| Input Voltage | 250 V - 400 V |
| Output Voltage | 12 V |
| Maximum Output Current | 80 A |
| Maximum Output Power | 1 kW |
| Switching Frequency | 170 – 250 kHz |
| Transformer Turns Ratio | 18 : 1 : 1 (center tapped) |
| Series Resonant Inductor | 13.4 µH (Ph1) - 12.5 µH (Ph2) |
| Parallel Resonant Inductor | 239 µH (Ph1) – 245.6 µH (Ph2) |
| Series Resonant Capacitor | 20 nF ± 5% |
| Parallel Resonant Capacitor | 5 nF ± 5% |
| SCC Capacitor (Each Phase) | 16.5 nF ± 5% |
| Input Capacitor | 136 µF ± 5% |
| Output Capacitor | 940 µF ± 5% |

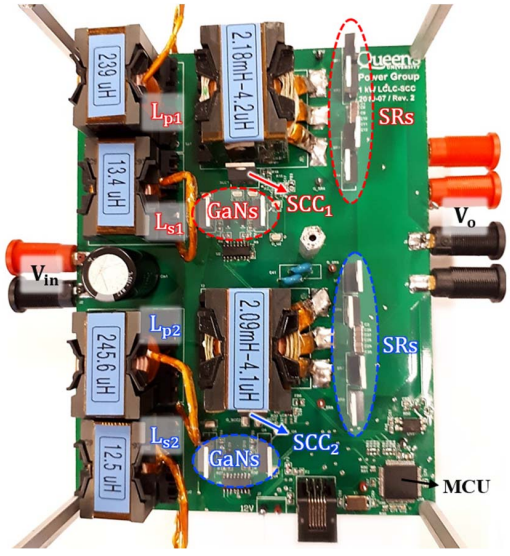


Fig. 10. A top-view of the implemented laboratory prototype.

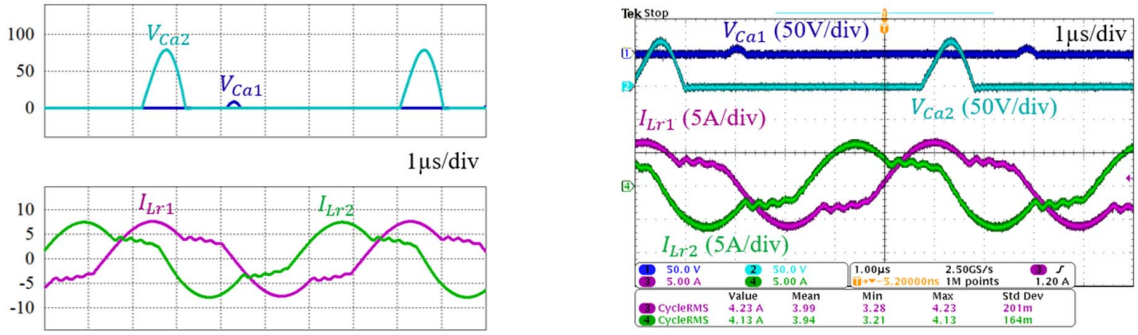



Fig. 11. Steady-state simulation (left column) and experimental (right column) results with $V_{in}$=250 V and $I_o$=70 A.

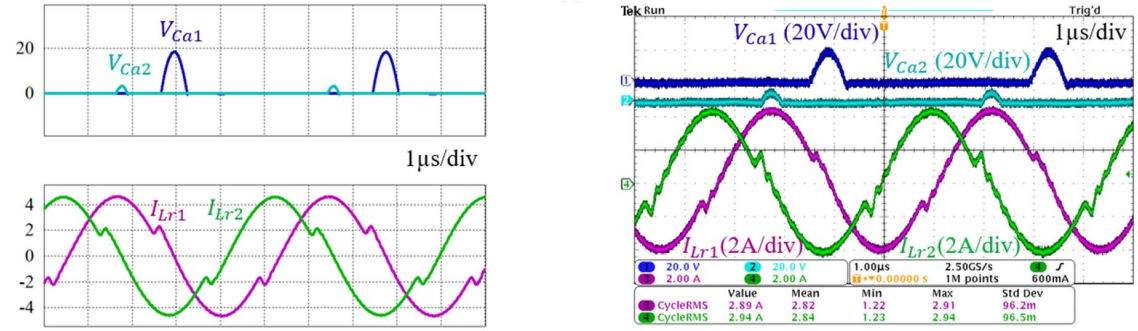



Fig. 12. Steady-state simulation (left column) and experimental (right column) results with $V_{in}$=400 V and $I_o$=80 A.

currents and SCC capacitor voltages with $V_{in}$=250 V at the full-load. As mentioned before, the required compensation by the SCC circuit is the largest around peak voltage gain and hence the SCC capacitor voltage ($V_{Ca}$) in phase 2 is around 75 V to compensate for lower voltage gain in phase 2 (see Fig. 4). Fig. 12 illustrates the steady-state results with $V_{in}$=400 V for the full-load condition. In this case, $V_{Ca}$ for both phases is below 20 V and as expected from Fig. 4 the SCC capacitor voltage is larger on phase 1. This is mainly because the voltage gains of two phases are close and near the resonant frequency, and hence less gain compensation is required by the SCC circuit around the resonant frequency. It can be observed from Fig. 11 and Fig. 12 that the SCC circuit is actively balancing the resonant current between both phases for both high and low input voltage conditions and there is a good consistency between the simulation and experimental results. Moreover, as desired by the control method, in both cases the α angle of the higher current carrying phase is always kept at the maximum α angle (i.e. 170º here) to reduce the asymmetric effect due to SCC operation. Moreover, even for a large imbalance that is occurring with 250 V input voltage, the SCC voltage rating is below 100 V that allows low drain-source on-resistance MOSFET ($R_{DS(on)}$ =3-5mΩ) implementation for the SCC circuit, which brings negligible conduction loss.

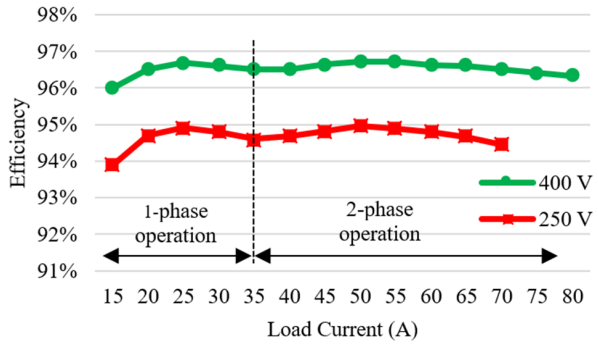



Fig. 13. Measured efficiency curves considering phase shedding with $V_{in}$=250 V and $V_{in}$=400 V conditions.

Fig. 13 illustrates the measured efficiency curves of the interleaved LCLC converter after considering phase shedding for $V_{in}$=250 V with red color and for $V_{in}$=400 V with green color. It is shown that the implemented LCLC converter has a flat efficiency profile with both input voltages. Moreover, with a nominal input voltage, the efficiency is over 96 % from 15 A to 80 A and the maximum efficiency is 96.7 %.

## V. Conclusion

This paper provides current balancing analysis and control of a two-phase interleaved LCLC resonant converter for wide input voltage range applications. A precise current balancing is obtained by employing two SCC circuits in both phases of the interleaved LCLC resonant converter. An abnormal voltage gain imbalance condition is studied on the interleaved LCLC converter and the current sharing analysis revealed that a minimum operating angle is necessary for the SCC circuit to have a reliable performance. The current sharing performance is verified through both computer simulation and experimental results for $V_{in}$=250 V and $V_{in}$=400 V conditions. Moreover, a

flat efficiency curve between 20 % to 100 % load is obtained with a maximum efficiency of 96.7 %.

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